GROWTH AND CHARACTERIZATION OF HIGH-Ge CONTENT SiGe VIRTUAL SUBSTRATES

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$Si_{1-x}Ge_x$ virtual substrates with relaxed graded buffers grown in industrial LPCVD reactors on 150 mm and 200 mm diameter wafers are presented with compositions up to $x = 1$. By taking advantage of an intermediate planarization step, we are able to achieve dislocation glide limited relaxation throughout the growth of the entire graded buffer layer. This resulted in a threading dislocation density of 2×10^5 cm^{-2} that was independent of the ultimate composition for substrates with $x > 0.4$. Ge-on-Si virtual substrates exhibited an rms surface roughness of 3.27 nm for a 20 μm × 20 μm area and a very low density of epitaxial defects. These substrates were used to fabricate both III-V solar cells and visible LEDs. The preliminary results of the devices showed no degradation in device performance from the graded buffer layer, demonstrating the commercial readiness of the SiGe virtual substrates.

INTRODUCTION

The SiGe virtual substrate is a platform that is capable of enhancing the performance and expanding the capabilities of the ubiquitous Si substrate. Strained Si CMOS is the predominant application for $Si_{1-x}Ge_x$ virtual substrates with low Ge content, $x < 0.4$ [1]–[3]. For higher Ge content, $x > 0.4$, additional applications are realized, such as dual-channel, ultra-high mobility strained Si CMOS [4] and III-V/Si monolithic integration [5].

In order to serve as a high-quality substrate for commercial applications, the SiGe virtual substrate must have (i) as low a threading dislocation density as possible, (ii) as low a surface roughness as possible, (iii) be fully relaxed throughout the structure, and (iv) be available in the commercial diameters of 150 mm, 200 mm, and 300 mm. One of the most widely reported techniques used to meet these criteria is the relaxed compositionally graded $Si_{1-x}Ge_x$ buffer layer [6] that can cover the entire compositional range of $x = 0\rightarrow1$.

The essential quality of the relaxed graded buffer layer is its ability to relieve lattice mismatch strain without additional dislocation nucleation. By gradually increasing the lattice constant throughout the growth, strain is introduced into the top layer at a steady rate that facilitates the glide of existing threading dislocations. As they glide, the threading dislocations leave misfit dislocations in their wake that relax the bottom layers. Provided that the density of threading dislocations is sufficient and their glide velocity is sufficient, the relaxation process should continue without the need to nucleate more threading dislocations. This should also hold true regardless of the ultimate graded buffer layer composition.

If the glide velocity of the threading dislocations slows down, however, then the misfit dislocations that they extend will no longer be adequate to relax fully the bottom layers. To accommodate the leftover strain, new threading dislocations must be nucleated. For the case of SiGe, the main cause of velocity impediment is the presence of surface roughness that is manifested by the characteristic orthogonal crosshatch pattern.

The undulations of the crosshatch are a result of inhomogeneous strain fields accumulated from buried misfit dislocations. The strain fields affect localized growth rates, which become slower in areas of higher strain. The troughs of the crosshatch can become deep enough that it can stop the glide of a threading dislocation entirely. Immobile threading dislocations in these regions can pin other threading dislocations to form dislocation pile-ups. A direct correlation was found between the surface roughness and pile-up density as well as the surface roughness and total threading dislocation density [7].

To reduce the surface roughness of the SiGe graded buffer layer, a planarization step is added during the growth sequence [8]. This liberates the threading dislocations pinned in pile-ups by removing their inability to glide. Thus not only are existing pile-ups eliminated by the planarization step, but the formation of future pile-ups are inhibited due to the sharply reduced surface roughness. As a result, the unimpeded glide velocity of the threading dislocations is restored, and the subsequent growth of the SiGe graded buffer layer can continue with low threading dislocation density, low surface roughness, and full relaxation.

Taking advantage of the benefits of graded layer epitaxy and planarization, we have grown high-quality, 150 and 200 mm diameter $Si_{1-x}Ge_x$ virtual substrates with ultimate compositions up to $x = 1$ with commercial low-pressure chemical vapor deposition (LPCVD) techniques. The growth sequence is divided into three steps:

1. The growth of the initial $Si_{1-x}Ge_x$ relaxed graded buffer layer from $x = 0\rightarrow0.4$
2. The planarization of the substrate by chemical mechanical polishing (CMP)
3. The regrowth of the $Si_{1-x}Ge_x$ graded buffer layer from $x = 0.4\rightarrow0.9$.

Using this sequence, we were able to maintain a constant threading dislocation density of $\sim2\times10^5$ cm^{-2} for ultimate compositions up to $x = 0.9$. In addition, Ge-on-Si virtual substrates were created with the addition of a Ge cap layer. The rms surface roughness for these substrates is 3.27 nm for a 20 μm × 20 μm scan area.

The SiGe virtual substrates created in this work are able to meet, for the first time,

the demands listed above of commercial applications, namely low threading dislocation density, low surface roughness, full relaxation, and large diameter availability. To highlight applications of the Ge-on-Si virtual substrates, we demonstrate preliminary results for III-V solar cells fabricated at both commercial and institutional facilities and visible light emitting diodes.

EXPERIMENT

All epitaxy of the SiGe virtual substrates took place in industrial LPCVD reactors. SiH_4 and GeH_4 were the source gases for Si and Ge, and B_2H_6 and PH_3 served as the *p*-type and *n*-type dopants, respectively. The growth temperature varied between 700 and 1000°C and was incrementally lowered with increasing Ge content. The growth rate varied between 50 and 200 nm/min and depended strongly on the SiH_4:GeH_4 flow rate ratio.

The (100) Si substrates have a 6° intentional miscut toward the in-plane <110> direction to suppress anti-phase boundary formation [9] that occurs during III-V epitaxy on the Ge-on-Si virtual substrates. To facilitate device fabrication, the entire virtual substrate growth was doped either *p*-type on p^+ Si substrates or *n*-type on n^+ Si substrates. Both 150 mm and 200 mm diameter Si substrates were used in this study.

The $Si_{1-x}Ge_x$ buffer layers were linearly graded at a rate of $x = 0.1$ μm^{-1} using 0.2 μm-thick constant composition steps incremented by $x = 0.02$. The linear grade proceeded until $x = 0.4$, at which point a 1.5 μm-thick $Si_{0.6}Ge_{0.4}$ layer was deposited. The planarization by CMP occurred next, which removed approximately 0.5 μm of material from the top layer. The planarized substrate was inserted back into the reactor for the regrowth step, where linear grading to the ultimate composition continued followed by the deposition of a 1.5 μm-thick cap layer.

The threading dislocation density was revealed primarily by etch pit density (EPD) measurements. Since a variety of virtual substrate compositions and dopant types were studied, we verified the values obtained by EPD with those by plan-view transmission electron microscopy (PVTEM). The composition and relaxation of the SiGe graded buffer layer was determined by triple-axis x-ray diffraction, while the surface roughness was determined by atomic force microscopy (AFM). Visual inspection was aided by Nomarski optical microscopy.

RESULTS AND DISCUSSION

We performed a systematic study to determine the effects of planarization on the threading dislocation density of $Si_{1-x}Ge_x$ virtual substrates for a variety of compositions. For the virtual substrates with $x < 0.4$, only the first step of the growth sequence was performed up to the ultimate composition. When $x \geq 0.4$, all three steps were performed, with the regrowth step continuing to the ultimate composition. The threading dislocation density of various virtual substrates up to $x = 0.9$ is shown in Fig. 1 as a function of the ultimate composition. For $x = 0.2$–0.3, the density is ~1×10^5 cm^{-2}, and for $x = 0.4$–0.9, the density is ~2×10^5 cm^{-2}. A constant threading dislocation density is maintained for these virtual substrates despite a variation in mismatch from 0.8 to 3.7% and total nominal graded buffer layer thickness from 3.5 to 11.5 μm as x is increased from 0.2 to 0.9. To our knowledge, this is the first observation of this phenomenon.

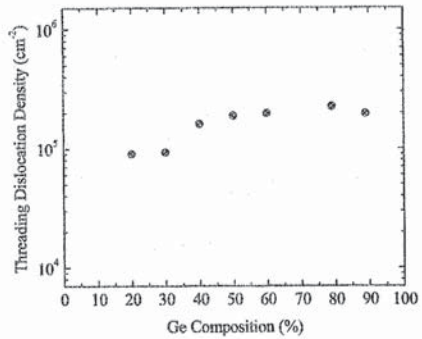

FIG. 1. The threading dislocation density of various $Si_{1-x}Ge_x$ virtual substrates as a function of the ultimate composition. The density is nearly held constant at ~2×10^5 cm^{-2} for compositions up to $x = 0.9$.

Assuming that the relaxation of the SiGe graded buffer layers is dislocation glide limited and not dislocation nucleation limited, the threading dislocation density ρ_t can be empirically expressed as [10]

$$\rho_t \propto R_g R_{gr} \exp(U/kT) \qquad (1)$$

where R_g is the growth rate, R_{gr} is the compositional grading rate, U is the dislocation glide activation energy, k is Boltzmann's constant, and T is the growth temperature. Thus for ideal dislocation guide limited relaxation, the threading dislocation density varies only with user-controlled parameters: growth rate, grading rate, and growth temperature. There is no dependence on the ultimate composition, total mismatch, or total thickness.

Because the SiGe virtual substrates with $x > 0.4$ have a composition-independent threading dislocation density and were grown with identical growth conditions, they exhibit ideal dislocation glide limited relaxation. This points to the importance of the intermediate planarization step—the surface roughnesses of a $Si_{0.6}Ge_{0.4}$ virtual substrate before and after planarization are 10.1 nm and 0.62 nm, respectively, for a 30 μm × 30 μm scan area. By releasing pile-ups, the impediments to glide velocity are removed. It also points to the importance of carefully controlling the growth conditions, so that the glide velocity is maintained, even for higher compositions. We observe by EPD that the regrowth step creates very few pile-ups, and as a result, the relaxation is still allowed to be glide limited even when $x = 0.9$.

Previous work [11] in $Si_{1-x}Ge_x$ graded buffer layers also reported dislocation glide limited relaxation, but for higher compositions, $x > 0.3$, a large jump in the threading

dislocation density occurred. This was accompanied by the onset of pile-up formation, which acted as barriers to dislocation glide. As the number of threading dislocations pinned in pile-ups increased, the number of threading dislocations nucleated increased. Without a method of controlling the pile-ups, such as an intermediate planarization step, the total threading dislocation density would continue to rise unabatedly.

To create Ge-on-Si virtual substrates, we deposit a thin, typically 0.2–1.0 μm, Ge cap layer directly on $Si_{0.1}Ge_{0.9}$ virtual substrates. The abrupt jump in composition between $x = 0.9$ and 1 is inserted to offset the thermal mismatch between Ge and Si [8]. Ge has a larger thermal coefficient of expansion than Si at all temperatures ($\alpha_{Ge} = 5.75\times10^{-6}$ K^{-1} and $\alpha_{Si} = 2.33\times10^{-6}$ K^{-1} at 300 K), so as the substrate is cooled down to room temperature following epitaxy, the Ge-rich layers develop tensile strain. By depositing the Ge layer with a slight compressive strain, the thermal mismatch stress is countered. Fig. 2 contains a 20 μm × 20 μm AFM scan of a Ge-on-Si virtual substrate. The effect of the 6° toward <110> off-cut is seen in the crosshatch pattern, which causes the misfit dislocations to lie 6° away from the apparent [110] direction but parallel to the [$\bar{1}$10] direction [12]. For a 20 μm × 20 μm area, the average rms surface roughness is 3.27 nm.

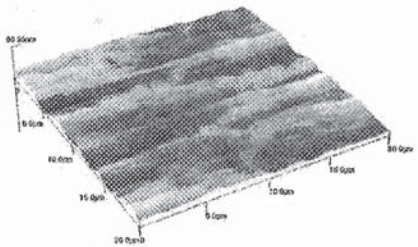

FIG. 2. A 20 μm × 20 μm AFM scan of a Ge-on-Si virtual substrate. The surface undulations, due to crosshatch, deviate from the orthogonal <110> directions because of the 6° toward <110> off-cut of the (100) Si substrate. For a 20 μm × 20 μm area, the average rms surface roughness is 3.27 nm.

Figs. 3(a) and (b) contain Nomarski optical micrographs of Ge-on-Si virtual substrates before and after optimization of each of the three steps of the growth sequence. The crosshatch is less pronounced in (b), indicating a lower surface roughness. Also, the density of large area epitaxial defects, speculated to be caused by gas-phase nucleation, is decreased in (b). These defects appear as spade-shaped pits in the images. If deep enough, they will affect the electrical characteristics of devices fabricated on these substrates by acting as shunts through the device structure.

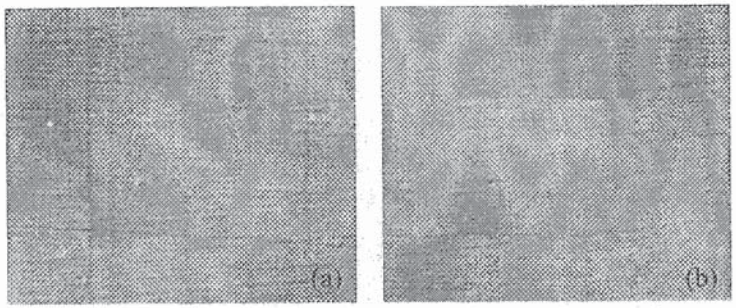

FIG. 3. Nomarski optical micrographs of Ge-on-Si virtual substrates (a) before and (b) after optimization of the growth sequence. The spade-shaped pits are epitaxial defects that, if deep enough, may affect the electrical characteristics of devices fabricated on these substrates. The image sizes are (a) 210 μm × 175 μm and (b) 525 μm × 437 μm.

Fig. 4 shows an asymmetric {224} reciprocal space map of a Ge-on-Si virtual substrate collected by triple-axis x-ray diffraction; it is shown in logarithmic scale representing 3.2 orders of magnitude. The entire $Si_{1-x}Ge_x$ graded buffer layer from $x = 0\rightarrow1$ is revealed. Four main peaks are observed: the Si substrate, the intermediate $Si_{0.6}Ge_{0.4}$ cap layer grown before planarization, the $Si_{0.1}Ge_{0.9}$ graded buffer cap layer, and the Ge cap layer. The predominant orientation of broadening of the last three peaks is perpendicular to the origin line, indicating that there is some degree of mosaic tilting inside the layer due to the effect of the misfit dislocations. A faint secondary peak near the $Si_{0.6}Ge_{0.4}$ peak shows that the composition of the initial graded buffer layer regrowth after CMP is slightly off by $x \approx 0.01$. By collecting a second {224} reciprocal space map with the substrate rotated around the azimuth by 180°, the effect of epilayer tilt on the measurement is eliminated and the composition and relaxation for each layer can be calculated. For this particular virtual substrate, the entire graded buffer layer from $x = 0\rightarrow0.9$ is fully relaxed, and the Ge cap layer is 90% relaxed.

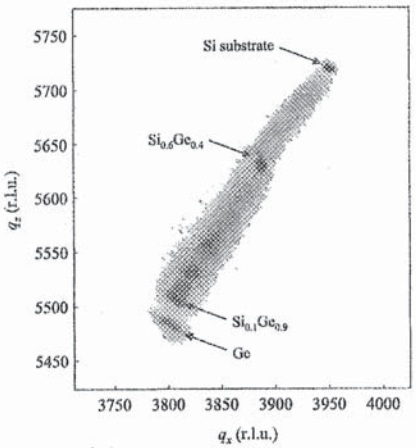

FIG. 4. An asymmetric {224} reciprocal space map of a Ge-on-Si virtual substrate collected by triple-axis x-ray diffraction. The four main peaks are labeled, corresponding to the Si substrate, the intermediate $Si_{0.6}Ge_{0.4}$ cap layer grown before planarization, the $Si_{0.1}Ge_{0.9}$ graded buffer cap layer, and the Ge cap layer.

APPLICATIONS

Solar cells

Unlike the direct epitaxy of GaAs on Si, the relatively low threading dislocation densities achieved by Ge-on-Si virtual substrates allows them to act as sufficient templates to enable the high minority carrier lifetimes required for high efficiency solar cells for space-based applications. Previous work [13] demonstrated a high minority carrier lifetime of 10 ns and an open circuit voltage of 1040 mV for p/n single junction GaAs solar cells on Ge-on-Si virtual substrates under AM0 conditions. Yet due to a high density of large area epitaxial defects, seen in Fig. 3(a), these devices were limited to small area cells, 0.2 cm × 0.2 cm. With the decreased large area epitaxial defect density available in our Ge-on-Si virtual substrates, as imaged above in Fig. 3(b), larger area single junction GaInP/GaAs solar cells were able to be fabricated.

Our first attempt to grow a GaInP/GaAs solar cell structure on a Ge-on-Si virtual substrate at a commercial solar cell facility resulted in thermally induced cracking in the epitaxial structure. Growth of III-V solar cells structures on Ge-on-Si substrates is susceptible to cracking because of the relatively thick films required for photon collection; a total of approximately 4.4 μm of III-V growth was required by the current cell design. This cracking is pictured in Fig. 5(a); the arrows point to the linear cracks. Refinements to the process resulted in solar cells free of cracks, pictured in Fig. 5(b).

These included adjustments to the thermal budget and design of the solar cell.

As a result, large area III-V solar cell structures were produced. The crack-free III-V growth also showed no evidence of anti-phase boundaries or other major defects such as stacking faults. Solar cells having areas of 2 cm × 2 cm were then fabricated and tested. The cells exhibited an open circuit voltage of 860 mV, a fill factor of 72.4%, and a short circuit current of 22.2 mA/cm^2. These values were lower than expected due to problems with the anti-reflection coating deposition and the need for further refinements in the cell growth process. However, these initial tests indicate that the Ge-on-Si virtual substrates are a viable substrate platform for commercial solar cell processes.

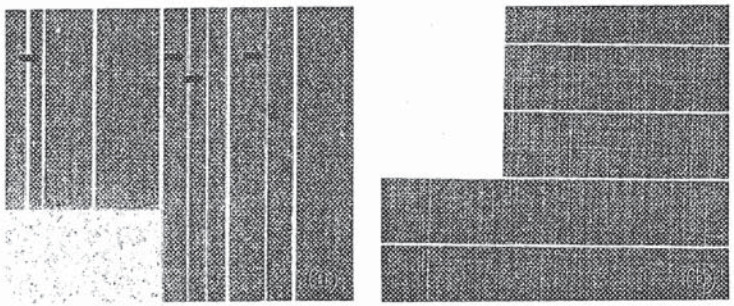

FIG. 5. The metal contact region (light colored areas) of 2 cm × 2 cm solar cells (a) before and (b) after process optimization. Optimization of the III-V growth process resulted in the elimination of thermally induced cracking. The narrow lines in (a) identified by the arrows are cracks; the thicker lines are the metal contact fingers. The images are 1050 μm × 874 μm.

Single junction GaInP/GaAs solar cells were also fabricated at an institutional solar cell research facility. High quality III-V growth was also achieved during this phase of testing, including crack-free, APB-free growth. Both p/n and n/p solar cell structures were used. The n/p cell structures are more sensitive to the detrimental impact of threading dislocations than a p/n cell structure [14]. The reason for this is that the minority carrier diffusion length of electrons in the n/p cell's base region is longer than for holes in the p/n cell's base region. Consequently, electrons are more likely to encounter a threading dislocation prior to reaching the collector region. The relatively low threading dislocation density of the current Ge-on-Si virtual substrate allows for the evaluation of the more commercially representative n/p structure.

The scalability of the solar cell area was demonstrated as shown in Figs. 6 and 7. The open circuit voltage showed zero reduction as the cell area was increased. For p/n structures, the open circuit voltage was 936 mV for both 0.4 cm × 0.4 cm and 0.6 cm × 0.6 cm cell areas. For n/p structures, the open circuit voltage was 906 mV for both 0.4 cm × 0.4 cm and 0.6 cm × 0.6 cm cell areas. The fill factors were slightly reduced from

74.5% to 71.4% for p/n structures and from 75.2% to 74.6% for n/p structures as the cell area was increased from 0.4 cm × 0.4 cm to 0.6 cm × 0.6 cm. Larger 2 cm × 2 cm cells with p/n structures were also produced. The open circuit voltage was 875 mV, the fill factor was 48.9%, and the short circuit current was 27.9 mA/cm^2. Unfortunately, the performance of these cells was degraded by a problem fabricating the backside contact.

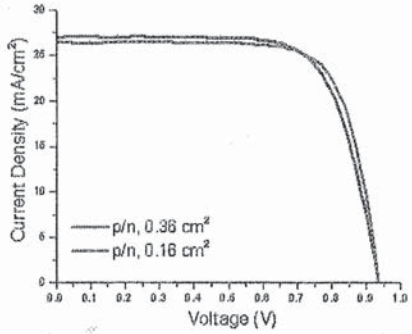

FIG. 6. The illuminated I-V response under AM0 conditions for single junction GaInP/GaAs/Ge-on-Si p/n cells of two different areas. Both cells have identical open circuit voltages.

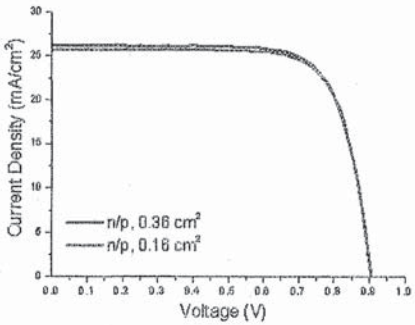

FIG. 7. The illuminated I-V response under AM0 conditions for single junction GaInP/GaAs/Ge-on-Si n/p cells of two different areas. Both cells have identical open circuit voltages.

These solar cells also were not optimized with respect to the solar cell structure and fabrication. Nevertheless, for the purpose of evaluating the viability of using the Ge-on-Si virtual substrate for solar cells, the scalability of the cell area is promising. While the performance of the solar cells was lower than previously published data, we were able to increase the cell area by a factor of 100. Further refinements to the solar cell fabrication will certainly enhance both the device performance and cell area.

Visible LEDs

The low threading dislocation density of the commercially fabricated Ge-on-Si virtual substrate also allows the realization of light emitting diodes (LEDs) and lasers. GaAs-based near-infrared lasers were recently demonstrated on Ge-on-Si virtual substrates [15]. Visible emitters monolithically integrated on Si can be used in chip-to-chip communication modules or short-haul local area networks.

GaInP/AlGaInP/GaAs LEDs were fabricated directly on Ge-on-Si substrates with top and bottom contacts. The emitter structure epitaxy proceeded without cracking. The L-I-V curve of an LED emitting at a peak wavelength of 660 nm is pictured in Fig. 8. The output power of the 110 μm × 1100 μm device is 0.6 μW at a current of 20 mA. The turn-on voltage is 1.54 V, and the device resistance is 6.5 Ω.

Although the light emission of the device is not optimized, it possesses very good electrical characteristics, as evidenced by the turn-on voltage and device resistance. An identical LED fabricated on a Ge substrate had a turn-on voltage of 1.53 V and a total resistance of 4.8 Ω, so the SiGe graded buffer layer structure did not degrade the electrical characteristics.

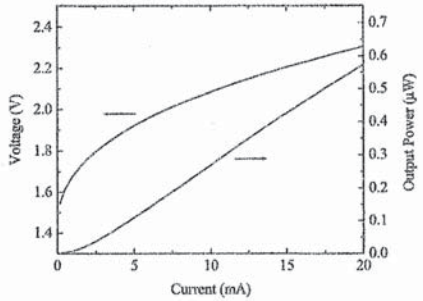

FIG. 8. The L-I-V curve of a AlGaInP/GaInP/GaAs LED fabricated on a Ge-on-Si virtual substrate. The peak emission wavelength is 660 nm and the device dimensions are 110 μm × 1100 μm.

CONCLUSION

We have demonstrated the commercial fabrication of high-quality $Si_{1-x}Ge_x$ virtual substrates with ultimate compositions up to $x = 1$ by LPCVD. Through deliberate control of the growth conditions and planarization, dislocation glide limited relaxation is observed in these fully-relaxed substrates for all compositions studied up to $x = 0.9$. As

such, the threading dislocation density is maintained at 2×10^5 cm^{-2} for virtual substrates with $x > 0.4$. At the same time, the low surface roughness of the virtual substrates is sustained, accompanied by a very low density of epitaxial defects. Ge-on-Si virtual substrates, created by depositing a thin Ge layer directly on $Si_{0.1}Ge_{0.9}$ substrates, have an rms surface roughness of 3.27 nm. The 150 mm and 200 mm diameter SiGe virtual substrates created in this work have met the demands of commercial applications. To demonstrate some of these applications, the Ge-on-Si virtual substrates were used to fabricate both III-V solar cells and visible LEDs. The solar cells were created at both commercial and institutional facilities. The preliminary results show no reduction in open circuit voltage and only a slight reduction in fill factor for increasing cell area. Cell areas as large as 2 cm × 2 cm were achieved, which is 100 times larger than previously reported solar cells on Ge-on-Si virtual substrates. The LEDs successfully operated in the visible wavelength region, and there was no degradation in its electrical characteristics when compared to similar LEDs on Ge substrates. These applications show the strength of SiGe virtual substrates as a platform for advanced microelectronic and optoelectronic integration.

ACKNOWLEDGMENTS

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